Amendments to the Specification:

Please replace the Brief Description of the Drawings section with the following:

–BRIEF DESCRIPTION OF THE DRAWINGS

The drawings for this patent are the same as those in U.S. Pat. No. 6,130,602, which has been incorporated by reference. ~~Preferred embodiments of the invention are described below with reference to the following accompanying drawings. Like names for circuit blocks indicate like components. Where there are a plurality of identical circuit blocks, detailed drawings are provided for one such circuit block. Some circuit schematics have been numbered in a hierarchial manner to reflect the hierarchial nature of these drawings. Notwithstanding the order in which the figures are numbered, note that some detailed drawings provide details to blocks included in more than one higher level drawing. Some circuit schematics have been broken up into many portions due to size requirements for patent drawings.~~

~~Fig. 1 is a high level circuit schematic showing a circuit embodying the invention.~~

~~Fig. 2 is a front view of an employee badge according to but one embodiment the invention.~~

~~Fig. 3 is a front view of a radio frequency identification tag according to another embodiment of the invention.~~

~~Fig. 4 is a block diagram of an electronic identification system according to the invention and including an interrogator and the tag of Fig. 3.~~

~~Fig. 5 is a high level circuit schematic of a monolithic semiconductor integrated circuit utilized in the devices of Figs. 1-4.~~

~~Fig. 6 is a graph illustrating how Figs. 6AA-EK are to be assembled. After such assembly, Figs. 6AA-EK provide a circuit drawing of another high level circuit schematic of the monolithic semiconductor integrated circuit of Fig. 5, showing pads and other details.~~

~~Fig. 6.01 is a layout diagram illustrating the physical layout of various components on an integrated circuit die, in accordance with one embodiment of the invention. The physical locations and sizes of components relative to other components are shown. Boundaries between various blocks may be approximate in the sense that portions of certain blocks may extend into other blocks.~~

~~Fig. 7 is a graph illustrating how Figs. 7AA-HJ are to be assembled. After such assembly, Figs. 7AA-HJ provide a circuit drawing of a data processor "dataproc" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 7.01 is a graph illustrating how Figs. 7.01AA-BB are to be assembled. After such assembly, Figs. 7.01AA-BB provide a circuit drawing of a processor clock generator "clk" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0101 is a graph illustrating how Figs. 7.0101AA-BB are to be assembled. After such assembly, Figs. 7.0101AA-BB provide a circuit drawing of a processor clock controller "clkctl" included in the circuit of Figs. 7.01AA-BB.~~

~~Fig. 7.0102 is a graph illustrating how Figs. 7.0102AE-DJ are to be assembled. After such assembly, Figs. 7.0102AE-DJ provide a circuit drawing of a phase generator "clkph" included in the circuit of Figs. 7.01AA-BB.~~

~~Fig. 7.0103 is a graph illustrating how Figs. 7.0103AA-BD are to be assembled. After such assembly, Figs. 7.0103AA-BD provide a circuit drawing of a state generator "clkst" included in the circuit of Figs. 7.01AA-BB.~~

~~Fig. 7.010301 is a graph illustrating how Figs. 7.010301AA-BB are to be assembled. After such assembly, Figs. 7.010301AA-BB provide a circuit drawing of a clock generator counter bit "clkcbit" included in the circuit of Figs. 7.0103AA-BD.~~

~~Fig. 7.02 is a graph illustrating how Figs. 7.02AA-BF are to be assembled. After such assembly, Figs. 7.02AA-BF provide a circuit drawing of an address decoder "adrdec" included in the circuit of Figs. 7AA-BF.~~

~~Fig. 7.03 is a graph illustrating how Figs. 7.03AA-EH are to be assembled. After such assembly, Figs. 7.03AA-EH provide a circuit drawing of a 512 byte RAM "ram" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0301 is a graph illustrating how Figs. 7.0301AA-BB are to be assembled. After such assembly, Figs. 7.0301AA-BB provide a circuit drawing of a RAM control circuit "ramctl" included in the circuit of Figs. 7.03AA-BB.~~

~~Fig. 7.0302 is a graph illustrating how Figs. 7.0302AA-AC are to be assembled. After such assembly, Figs. 7.0302AA-AC provide a circuit drawing of an 8x4 RAM array "ram8x4" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.030201 is a circuit drawing of a six transistor RAM cell "ramcell" included in the circuit of Figs. 7.0302AA-AC.~~

~~Fig. 7.0303 is a graph illustrating how Figs. 7.0303AA-AD are to be assembled. After such assembly, Figs. 7.0303AA-AD provide a circuit drawing of a RAM precharge circuit "rampch" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0304 is a graph illustrating how Figs. 7.0304AA-AD are to be assembled. After such assembly, Figs. 7.0304AA-AD provide a circuit drawing of a second RAM precharge circuit "ramdch" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0305 is a circuit drawing of a RAM address buffer "ramadb" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0306 is a graph illustrating how Figs. 7.0306AA-BA are to be assembled. After such assembly, Figs. 7.0306AA-BA provide a circuit drawing of a RAM word line driver "ramwdr" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0307 is a graph illustrating how Figs. 7.0307AA-BB are to be assembled. After such assembly, Figs. 7.0307AA-BB provide a circuit drawing of a RAM word line decoder "ramwdec" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0308 is a graph illustrating how Figs. 7.0308AA-BB are to be assembled. After such assembly, Figs. 7.0308AA-BB provide a circuit drawing of a RAM column select decode circuit "ramcdec" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0309 is a graph illustrating how Figs. 7.0309AA-BG are to be assembled. After such assembly, Figs. 7.0309AA-BG provide a circuit drawing of a RAM column selector "ramcsel" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.0310 is a graph illustrating how Figs. 7.0310AA-BB are to be assembled. After such assembly, Figs. 7.0310AA-BB provide a circuit drawing of a RAM databus interface "ramdb" included in the circuit of Figs. 7.03AA-EH.~~

~~Fig. 7.04 is a graph illustrating how Figs. 7.04AA-HJ are to be assembled. After such assembly, Figs. 7.04AA-HJ provide a circuit drawing of a ROM "rom" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0401 is a graph illustrating how Figs. 7.0401AA-BB are to be assembled. After such assembly, Figs. 7.0401AA-BB provide a circuit drawing of a ROM control logic circuit "romctl" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0402 is a graph illustrating how Figs. 7.0402AA-AB are to be assembled. After such assembly, Figs. 7.0402AA-AB provide a circuit drawing of a ROM bit line precharge circuit "rompch" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0403 is a graph illustrating how Figs. 7.0403AA-BB are to be assembled. After such assembly, Figs. 7.0403AA-BB provide a circuit drawing of a ROM word line driver "romwdr" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0404 is a graph illustrating how Figs. 7.0404AB-DC are to be assembled. After such assembly, Figs. 7.0404AA-DC provide a circuit drawing of a ROM word block decoder "romwdec_rev" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0405 is a graph illustrating how Figs. 7.0405AA-BA are to be assembled. After such assembly, Figs. 7.0405AA-BA provide a circuit drawing of a ROM bit line address driver "rombldr" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0406 is a graph illustrating how Figs. 7.0406AA-CK are to be assembled. After such assembly, Figs. 7.0406AA-CK provide a circuit drawing of a ROM bit line decoder "rombldec" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.0407 is a graph illustrating how Figs. 7.0407AA-AB are to be assembled. After such assembly, Figs. 7.0407AA-AB provide a circuit drawing of a ROM sense amplifier "romsns" included in the circuit of Figs. 7.04AA-HJ.~~

~~Fig. 7.05 is a graph illustrating how Figs. 7.05AA-CB are to be assembled. After such assembly, Figs. 7.05AA-CB provide a circuit drawing of an instruction register "insreg" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0501 is a graph illustrating how Figs. 7.0501AA-AB are to be assembled. After such assembly, Figs. 7.0501AA-AB provide a circuit drawing of an instruction register cell "insreel" included in the circuit of Figs. 7.05AA-CB.~~

~~Fig. 7.06 is a graph illustrating how Figs. 7.06AA-CN are to be assembled. After such assembly, Figs. 7.06AA-CN provide a circuit drawing of an instruction decoder PLA "insdec" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0601 is a graph illustrating how Figs. 7.0601AA-HI are to be assembled. After such assembly, Figs. 7.0601AA-HI provide a circuit drawing of an instruction decoder "insdec1" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0602 is a graph illustrating how Figs. 7.0602AA-JH are to be assembled. After such assembly, Figs. 7.0602AA-JH provide a circuit drawing of an instruction decoder (second section) "insdec2" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0603 is a graph illustrating how Figs. 7.0603AA-JI are to be assembled. After such assembly, Figs. 7.0603AA-JI provide a circuit drawing of an instruction decoder (third section) "insdec3" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0604 is a graph illustrating how Figs. 7.0604AA-JI are to be assembled. After such assembly, Figs. 7.0604AA-JI provide a circuit drawing of an instruction decoder (fourth section) "insdec4" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.060401 is a circuit drawing of an instruction decoder ROM amp "insramp" included in the circuit of Figs. 7.0604AA-JI.~~

~~Fig. 7.060402 is a circuit drawing of an instruction decoder PLA amp "inspamp" included in the circuit of Figs. 7.0604AA-JI.~~

~~Fig. 7.060403 is a circuit drawing of an instruction decoder PLA latch "insplat" included in the circuit of Figs. 7.0604AA-JI.~~

~~Fig. 7.07 is a graph illustrating how Figs. 7.07AA-BB are to be assembled. After such assembly, Figs. 7.07AA-BB provide a circuit drawing of a conditional qualifier decoder "cqualdec" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.08 is a graph illustrating how Figs. 7.08AA-CA are to be assembled. After such assembly, Figs. 7.08AA-CA provide a circuit drawing of a databus latch/precharge circuit "dblatch" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.09 is a graph illustrating how Figs. 7.09AA-BF are to be assembled. After such assembly, Figs. 7.09AA-BF provide a circuit drawing of an arithmetic logic unit "alu" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.0901 is a graph illustrating how Figs. 7.0901AA-CE are to be assembled. After such assembly, Figs. 7.0901AA-CE provide a circuit drawing of an ALU low byte "alubytl" included in the circuit of Figs. 7.09AA-BF.~~

~~Fig. 7.090101 is a graph illustrating how Figs. 7.090101AA-AD are to be assembled. After such assembly, Figs. 7.090101AA-AD provide a circuit drawing of a bit "alubitl" included in the circuit of Figs. 7.0901AA-CE.~~

~~Fig. 7.09010101 is a circuit drawing of an ALU bit decoder cell "alubdec" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010102 is a circuit drawing of an ALU B register cell "alubcell" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010103 is a graph illustrating how Figs. 7.09010103AA-AB are to be assembled. After such assembly, Figs. 7.09010103AA-AB provide a circuit drawing of an ALU A register cell "aluacell" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010104 is a graph illustrating how Figs. 7.09010104AA-AB are to be assembled. After such assembly, Figs. 7.09010104AA-AB provide a circuit drawing of an ALU register cell "alupc" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010105 is a circuit drawing of an ALU register cell "alurcell" included in the circuit of Figs. 7.090101AA-AD. Such register cells are used for a stack pointer and data pointer.~~

~~Fig. 7.09010106 is a graph illustrating how Figs. 7.09010106AA-AB are to be assembled. After such assembly, Figs. 7.09010106AA-AB provide a circuit drawing of an ALU memory address register "alumar" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010107 is a circuit drawing of an ALU slave cell "aluslave" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.09010108 is a graph illustrating how Figs. 7.09010108AA-BC are to be assembled. After such assembly, Figs. 7.09010108AA-BC provide a circuit drawing of an ALU adder "aluadd" included in the circuit of Figs. 7.090101AA-AD.~~

~~Fig. 7.0902 is a graph illustrating how Figs. 7.0902AA-BD are to be assembled. After such assembly, Figs. 7.0902AA-BD provide a circuit drawing of an ALU high byte "alubyth" included in the circuit of Figs. 7.09AA-BF.~~

~~Fig. 7.090201 is a graph illustrating how Figs. 7.090201AA-AC are to be assembled. After such assembly, Figs. 7.090201AA-AC provide a circuit drawing of a bit "alubith" included in the circuit of Figs. 7.09AA-BF.~~

~~Fig. 7.10 is a graph illustrating how Figs. 7.10AA-CC are to be assembled. After such assembly, Figs. 7.10AA-CC provide a circuit drawing of a timed lockout divider "tld" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1001 is a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of Figs. 7.10AA-CC.~~

~~Fig. 7.11 is a graph illustrating how Figs. 7.11AA-AB are to be assembled. After such assembly, Figs. 7.11AA-AB provide a circuit drawing of a timed lockout register "tloreg" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1101 is a graph illustrating how Figs. 7.1101AA-AC are to be assembled. After such assembly, Figs. 7.1101AA-AC provide a circuit drawing of a timed lockout register cell "tlorcel" included in the circuit of Figs. 7.11AA-AB.~~

~~Fig. 7.12 is a graph illustrating how Figs. 7.12AA-AC are to be assembled. After such assembly, Figs. 7.12AA-AC provide a circuit drawing of a R/W control register "oreg" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1201 is a circuit drawing of a R/W control register cell "regcell" included in the circuit of Figs. 7.12AA-AC.~~

~~Fig. 7.13 is a graph illustrating how Figs. 7.13AA-BA are to be assembled. After such assembly, Figs. 7.13AA-BA provide a circuit drawing of a status register "sreg" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1301 is a circuit drawing of a status register cell "sregcel" included in the circuit of Figs. 7.13AA-BA.~~

~~Fig. 7.14 is a graph illustrating how Figs. 7.14AA-AB are to be assembled. After such assembly, Figs. 7.14AA-AB provide a circuit drawing of a serial input/output block "sio" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1401 is a graph illustrating how Figs. 7.1401AA-GF are to be assembled. After such assembly, Figs. 7.1401AA-GF provide a circuit drawing of a serial input/output data path "siodata" included in the circuit of Figs. 7.14AA-AB.~~

~~Fig. 7.140101 is a graph illustrating how Figs. 7.140101AA-AB are to be assembled. After such assembly, Figs. 7.140101AA-AB provide a circuit drawing of a serial input/output register cell "sioreg" included in the circuit of Figs. 7.1401AA-AB.~~

~~Fig. 7.140102 is a circuit drawing of a serial input/output XOR circuit "sioxor" included in the circuit of Figs. 7.1401AA-GF.~~

~~Fig. 7.140103 is a graph illustrating how Figs. 7.140103AA-AB are to be assembled. After such assembly, Figs. 7.140103AA-AB provide a circuit drawing of a bidirectional latch "siobdlat_inv" included in the circuit of Figs. 7.1401AA-GF.~~

~~Fig. 7.140104 is a graph illustrating how Figs. 7.140104AA-AB are to be assembled. After such assembly, Figs. 7.140104AA-AB provide a circuit drawing of a shift register "sioshr" included in the circuit of Figs. 7.1401AA-GF.~~

~~Fig. 7.140105 is a graph illustrating how Figs. 7.140105AA-AB are to be assembled. After such assembly, Figs. 7.140105AA-AB provide a circuit drawing of a bidirectional latch "siobdlat" included in the circuit of Figs. 7.1401AA-GF.~~

~~Fig. 7.1402 is a graph illustrating how Figs. 7.1402BA-EI are to be assembled. After such assembly, Figs. 7.1402BA-EI provide a circuit drawing of serial input/output control logic "sioctl" included in the circuit of Figs. 7.14AA-AB.~~

~~Fig. 7.140201 is a graph illustrating how Figs. 7.140201AA-BB are to be assembled. After such assembly, Figs. 7.140201AA-BB provide a circuit drawing of a counter bit "siocbit" included in the circuit of Figs. 7.1402AA-AB~~

~~Fig. 7.15 is a graph illustrating how Figs. 7.15AA-EC are to be assembled. After such assembly, Figs. 7.15AA-EC provide a circuit drawing of a data interleaver (which interleaves two thirteen bit words) "dil" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1501 is a graph illustrating how Figs. 7.1501AA-CA are to be assembled. After such assembly, Figs. 7.1501AA-CA provide a circuit drawing of a data interleaver shift register "dil_sreg" included in the circuit of Figs. 7.15AA-EC.~~

~~Fig. 7.1502 is a graph illustrating how Figs. 7.1502AA-CA are to be assembled. After such assembly, Figs. 7.1502AA-CA provide a circuit drawing of a data interleaver shift register with parallel load "dil_plsreg" included in the circuit of Figs. 7.15AA-EC.~~

~~Fig. 7.150201 is a circuit drawing of a data interleaver shift register bit "dil_sregbit" included in the circuit of Figs. 7.1502AA-CA.~~

~~Fig. 7.16 is a graph illustrating how Figs. 7.16AA-CD are to be assembled. After such assembly, Figs. 7.16AA-CD provide a circuit drawing of a convolutional encoder and preamble generator "conv" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.1601 is a circuit drawing of a shift register cell "convshr" included in the circuit of Figs. 7.16AA-CD.~~

~~Fig. 7.1602 is a circuit drawing of a summer "convsum" included in the circuit of Figs. 7.16AA-CD.~~

~~Fig. 7.17 is a graph illustrating how Figs. 7.17AA-BB are to be assembled. After such assembly, Figs. 7.17AA-BB provide a circuit drawing of a shift register input data MUX "shdcel" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 7.18 is a graph illustrating how Figs. 7.18AA-CC are to be assembled. After such assembly, Figs. 7.18AA-CC provide a circuit drawing of a digital port output controller "doutport" included in the circuit of Figs. 7AA-HJ.~~

~~Fig. 8 is a graph illustrating how Figs. 8AA-CB are to be assembled. After such assembly, Figs. 8AA-CB provide a circuit drawing of an RF processor "rfproc" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 8.01 is a graph illustrating how Figs. 8.01AA-DE are to be assembled. After such assembly, Figs. 8.01AA-DE provide a circuit drawing of a receiver "rx" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.0101 is a graph illustrating how Figs. 8.0101AA-CB are to be assembled. After such assembly, Figs. 8.0101AA-CB provide a circuit drawing of a Schottky diode detector "diodedet" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0102 is a graph illustrating how Figs. 8.0102AA-BD are to be assembled. After such assembly, Figs. 8.0102AA-BD provide a circuit drawing of a CMOS square law detector "cmosdet" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0103 is a graph illustrating how Figs. 8.0103AA-CF are to be assembled. After such assembly, Figs. 8.0103AA-CF provide a circuit drawing of a video amplifier "videoamp1" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0104 is a graph illustrating how Figs. 8.0104AA-BC are to be assembled. After such assembly, Figs. 8.0104AA-BC provide a circuit drawing of a second video amplifier "videoamp2" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0105 is a graph illustrating how Figs. 8.0105AA-ED are to be assembled. After such assembly, Figs. 8.0105AA-ED provide a circuit drawing of a comparator "comparator" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0106 is a graph illustrating how Figs. 8.0106AA-CD are to be assembled. After such assembly, Figs. 8.0106AA-CD provide a circuit drawing of an RF detect circuit "rxdet" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0107 is a graph illustrating how Figs. 8.0107AA-GN are to be assembled. After such assembly, Figs. 8.0107AA-GN provide a circuit drawing of a receiver bias generator "rxbias" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.0108 is a graph illustrating how Figs. 8.0108AA-AC are to be assembled. After such assembly, Figs. 8.0108AA-AC provide a circuit drawing of a data transition detector "datatx" included in the circuit of Figs. 8.01AA-DE.~~

~~Fig. 8.02 is a graph illustrating how Figs. 8.02AA-BC are to be assembled. After such assembly, Figs. 8.02A-BC provide a circuit drawing of a low power frequency locked loop "lpfll" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.0201 is a graph illustrating how Figs. 8.0201AA-AB are to be assembled. After such assembly, Figs. 8.0201AA-AB provide a circuit drawing of a timed lockout divider cell "tldcel_bypass" included in the circuit of Figs. 8.02AA-BC.~~

~~Fig. 8.0202 is a graph illustrating how Figs. 8.0202AA-CD are to be assembled. After such assembly, Figs. 8.0202AA-CD provide a circuit drawing of a low power frequency locked loop frequency comparator "freqcomp" included in the circuit of Figs. 8.02AA-BC.~~

~~Fig. 8.0203 is a graph illustrating how Figs. 8.0203AA-BC are to be assembled. After such assembly, Figs. 8.0203AA-BC provide a circuit drawing of an up/down counter "udcounter" included in the circuit of Figs. 8.02AA-BC.~~

~~Fig. 8.020301 is a graph illustrating how Figs. 8.020301AA-BB are to be assembled. After such assembly, Figs. 8.020301AA-BB provide a circuit drawing of an adder "udcounter_adder" included in the circuit of Figs. 8.0203AA-BC.~~

~~Fig. 8.020302 is a graph illustrating how Figs. 8.020302AA-AB are to be assembled. After such assembly, Figs. 8.020302AA-AB provide a circuit drawing of a D type flip-flop "udcounter_dff" included in the circuit of Figs. 8.0203AA-BC.~~

~~Fig. 8.0204 is a graph illustrating how Figs. 8.0204AA-EJ are to be assembled. After such assembly, Figs. 8.0204AA-EJ provide a circuit drawing of a low power current controlled oscillator "lpcco" included in the circuit of Figs. 8.02AA-BC.~~

~~Fig. 8.0205 is a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of Figs. 8.02AA-BC.~~

~~Fig. 8.03 is a graph illustrating how Figs. 8.03AA-AB are to be assembled. After such assembly, Figs. 8.03AA-AB provide a circuit drawing of a counter bit "lpfll_cbit" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.04 is a graph illustrating how Figs. 8.04AA-EE are to be assembled. After such assembly, Figs. 8.04AA-EE provide a circuit drawing of a receiver wake up controller "rxwu" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.0401 is a graph illustrating how Figs. 8.0401AA-AB are to be assembled. After such assembly, Figs. 8.0401AA-AB provide a circuit drawing of wake up abort logic "wuabort" included in the circuit of Figs. 8.04AA-EE.~~

~~Fig. 8.040101 is a graph illustrating how Figs. 8.040101AA-AB are to be assembled. After such assembly, Figs. 8.040101AA-AB provide a circuit drawing of wake up abort logic counter bit "wuabort_cbit" included in the circuit of Figs. 8.0401AA-AB.~~

~~Fig. 8.0402 is a graph illustrating how Figs. 8.0402AA-AB are to be assembled. After such assembly, Figs. 8.0402AA-AB provide a circuit drawing of a timed lockout divider cell "tldcel" included in the circuit of Figs. 8.04AA-EE.~~

~~Fig. 8.05 is a graph illustrating how Figs. 8.05AA-DE are to be assembled. After such assembly, Figs. 8.05AA-DE provide a circuit drawing of a digital clock and data recovery circuit "dcr" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.0501 is a graph illustrating how Figs. 8.0501AA-BE are to be assembled. After such assembly, Figs. 8.0501AA-BE provide a circuit drawing of a PLL start-up circuit "dcr_startup" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.050101 is a graph illustrating how Figs. 8.050101AA-AB are to be assembled. After such assembly, Figs. 8.050101AA-AB provide a circuit drawing of a shift register cell "dcr_sreg" included in the circuit of Figs. 8.0501AA-BE.~~

~~Fig. 8.050102 is a graph illustrating how Figs. 8.050102AA-AB are to be assembled. After such assembly, Figs. 8.050102AA-AB provide a circuit drawing of a counter bit "dcr_counterbit" included in the circuit of Figs. 8.0501AA-BE.~~

~~Fig. 8.0502 is a graph illustrating how Figs. 8.0502AA-CD are to be assembled. After such assembly, Figs. 8.0502AA-CD provide a circuit drawing of a PLL state machine "dcr_statemachine" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.0503 is a graph illustrating how Figs. 8.0503AA-FN are to be assembled. After such assembly, Figs. 8.0503AA-FN provide a circuit drawing of a DCR bias generator "dcr_bias" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.0504 is a graph illustrating how Figs. 8.0504AA-EE are to be assembled. After such assembly, Figs. 8.0504AA-EE provide a circuit drawing~~

~~of a VCO control voltage generator "dcr_vcocontrol" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.050401 is a graph illustrating how Figs. 8.050401AA-CK are to be assembled. After such assembly, Figs. 8.050401AA-CK provide a circuit drawing of a coarse step generator "dcr_coarsestepgen" included in the circuit of Figs. 8.0504AA-EE.~~

~~Fig. 8.050402 is a graph illustrating how Figs. 8.050402AA-CJ are to be assembled. After such assembly, Figs. 8.050402AA-CJ provide a circuit drawing of a medium step generator "dcr_medstepgen" included in the circuit of Figs. 8.0504AA-EE.~~

~~Fig. 8.050403 is a graph illustrating how Figs. 8.050403AA-BI are to be assembled. After such assembly, Figs. 8.050403AA-BI provide a circuit drawing of a medium fine step generator "dcr_medfinestepgen" included in the circuit of Figs. 8.0504AA-EE.~~

~~Fig. 8.050404 is a graph illustrating how Figs. 8.050404AA-BB are to be assembled. After such assembly, Figs. 8.050404AA-BB provide a circuit drawing of a fine step controller "dcr_finestepctrl" included in the circuit of Figs. 8.0504AA-EE.~~

~~Fig. 8.050405 is a graph illustrating how Figs. 8.050405AA-EJ are to be assembled. After such assembly, Figs. 8.050405AA-EJ provide a circuit drawing of a fine step generator "dcr_finestepgen" included in the circuit of Figs. 8.0504AA-EE.~~

~~Fig. 8.0505 is a graph illustrating how Figs. 8.0505AA-EF are to be assembled. After such assembly, Figs. 8.0505AA-EF provide a circuit drawing of a receiver VCO "dcr_vco" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.0506 is a graph illustrating how Figs. 8.0506AA-BB are to be assembled. After such assembly, Figs. 8.0506AA-BB provide a circuit drawing of an RX clock generator "dcr_rxclkgen" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.050601 is a circuit drawing of an RX clock generator flip-flop "dcr_rxclkgenff" included in the circuit of Figs. 8.0506AA-BB.~~

~~Fig. 8.0507 is a graph illustrating how Figs. 8.0507AA-AB are to be assembled. After such assembly, Figs. 8.0507AA-AB provide a circuit drawing of a PLL non-overlapping clock generator "dcr_clkgen" included in the circuit of Figs. 8.05AA-DE.~~

~~Fig. 8.06 is a graph illustrating how Figs. 8.06AA-ED are to be assembled. After such assembly, Figs. 8.06AA-ED provide a circuit drawing of a BPSK/AM/Backscatter transmitter "tx" included in the circuit of Figs. 8AA-CB.~~

~~Fig. 8.0601 is a graph illustrating how Figs. 8.0601AA-BB are to be assembled. After such assembly, Figs. 8.0601AA-BB provide a circuit drawing of a transmitter PLL "txpllfsyn" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.060101 is a graph illustrating how Figs. 8.060101AA-CC are to be assembled. After such assembly, Figs. 8.060101AA-CC provide a circuit drawing of a TX phase/frequency detector "txpfdet" included in the circuit of Figs. 8.0601AA-BB.~~

~~Fig. 8.060102 is a graph illustrating how Figs. 8.060102AA-BB are to be assembled. After such assembly, Figs. 8.060102AA-BB provide a circuit drawing of a TX PLL charge pump "txchgpump" included in the circuit of Figs. 8.0601AA-BB.~~

~~Fig. 8.060103 is a graph illustrating how Figs. 8.060103AA-CB are to be assembled. After such assembly, Figs. 8.060103AA-CB provide a circuit drawing of a TX PLL loop filter "txloopfilter" included in the circuit of Figs. 8.0601AA-BB.~~

~~Fig. 8.060104 is a graph illustrating how Figs. 8.060104AA-DC are to be assembled. After such assembly, Figs. 8.060104AA-DC provide a circuit drawing of a TX VCO "txvco" included in the circuit of Figs. 8.0601AA-BB.~~

~~Fig. 8.06010401 is a graph illustrating how Figs. 8.06010401AA-BD are to be assembled. After such assembly, Figs. 8.06010401AA-BD provide a circuit drawing of a TX VCO stage "txvcostage" included in the circuit of Figs. 8.060104AA-DC.~~

~~Fig. 8.0601040101 is a graph illustrating how Figs. 8.0601040101AA-BC are to be assembled. After such assembly, Figs. 8.0601040101AA-BC provide a layout plot showing how the components of the VCO stage are laid out.~~

~~Fig. 8.060105 is a graph illustrating how Figs. 8.060105AA-DD are to be assembled. After such assembly, Figs. 8.060105AA-DD provide a circuit drawing of a divider "txdivider" included in the circuit of Figs. 8.0601AA-BB.~~

~~Fig. 8.06010501 is a graph illustrating how Figs. 8.06010501AA-AB are to be assembled. After such assembly, Figs. 8.06010501AA-AB provide a circuit drawing of a divider flip-flop "txdivtff" included in the circuit of Figs. 8.060105AA-DD.~~

~~Fig. 8.0602 is a graph illustrating how Figs. 8.0602AA-AB are to be assembled. After such assembly, Figs. 8.0602AA-AB provide a circuit drawing of a test mode data selector "txdatasel" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.0603 is a graph illustrating how Figs. 8.0603AA-AB are to be assembled. After such assembly, Figs. 8.0603AA-AB provide a circuit drawing of a BPSK modulation driver "txbpsk" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.0604 is a graph illustrating how Figs. 8.0604AA-AB are to be assembled. After such assembly, Figs. 8.0604AA-AB provide a circuit drawing of a frequency doubler "txdoubler" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.060401 is a graph illustrating how Figs. 8.060401AA-FE are to be assembled. After such assembly, Figs. 8.060401AA-FE provide a circuit drawing of a frequency doubler core "txfdbl" included in the circuit of Figs. 8.0604AA-ED.~~

~~Fig. 8.0605 is a graph illustrating how Figs. 8.0605AA-AB are to be assembled. After such assembly, Figs. 8.0605AA-AB provide a circuit drawing of a second frequency doubler "txdoubler2" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.060501 is a graph illustrating how Figs. 8.060501AA-CD are to be assembled. After such assembly, Figs. 8.060501AA-CD provide a circuit drawing of doubler driver amps "txfdbldrv" included in the circuit of Figs. 8.0605AA-CD.~~

~~Fig. 8.060502 is a graph illustrating how Figs. 8.060502AA-CD are to be assembled. After such assembly, Figs. 8.060502AA-CD provide a circuit drawing of second doubler driver amps "txfdbldrv2" included in the circuit of Figs. 8.0605AA-CD.~~

~~Fig. 8.060503 is a graph illustrating how Figs. 8.060503AA-FE are to be assembled. After such assembly, Figs. 8.060503AA-FE provide a circuit drawing of a frequency doubler core "txfdbl2" included in the circuit of Figs. 8.0605AA-CD.~~

~~Fig. 8.0606 is a graph illustrating how Figs. 8.0606AA-IE are to be assembled. After such assembly, Figs. 8.0606AA-IE provide a circuit drawing of a transmitter power amp "txpoweramp" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.0607 is a graph illustrating how Figs. 8.0607AA-JJ are to be assembled. After such assembly, Figs. 8.0607AA-JJ provide a circuit drawing of a transmitter bias generator "txbias" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.0608 is a graph illustrating how Figs. 8.0608AA-BB are to be assembled. After such assembly, Figs. 8.0608AA-BB provide a circuit drawing of a modulated backscatter transmitter "txmbs" included in the circuit of Figs. 8.06AA-ED.~~

~~Fig. 8.07 is a graph illustrating how Figs. 8.07AA-BB are to be assembled. After such assembly, Figs. 8.07AA-BB provide a partial circuit drawing of a 915 MHZ transmitter "tx915" included in the circuit of Figs. 8AA-CB in place of the transmitter "tx" in an alternative embodiment of the invention.~~

~~Fig. 8.0701 is a graph illustrating how Figs. 8.0701AA-CB are to be assembled. After such assembly, Figs. 8.0701AA-CB provide a circuit drawing of a TX VCO stage "txvcostage915" for use with the 915 MHZ transmitter "tx915" of Fig. 8.07 in place of the TX VCO "txvco" of Fig. 8.060104.~~

~~Fig. 9 is a graph illustrating how Figs. 9AA-CB are to be assembled. After such assembly, Figs. 9AA-CB provide a circuit drawing of an analog processor "anlgproc" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 9.01 is a graph illustrating how Figs. 9.01AA-DH are to be assembled. After such assembly, Figs. 9.01AA-DH provide a circuit drawing of an algorithmic A/D converter with databus interface "ada_new" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.0101 is a graph illustrating how Figs. 9.0101AA-CK are to be assembled. After such assembly, Figs. 9.0101AA-CK provide a circuit drawing of a differential I/O op-amp "dopamp" included in the circuit of Figs. 9.01AA-DH.~~

~~Fig. 9.0102 provides a circuit drawing of an analog divider (divide by two) "adaprescale" included in the circuit of Figs. 9.01AA-DH.~~

~~Fig. 9.0103 is a graph illustrating how Figs. 9.0103AJ-FP are to be assembled. After such assembly, Figs. 9.0103AJ-FP provide a circuit drawing of a control PLA "adactl_new" included in the circuit of Figs. 9.01AA-DH.~~

~~Fig. 9.010301 is a graph illustrating how Figs. 9.010301AA-CC are to be assembled. After such assembly, Figs. 9.010301AA-CC provide a circuit drawing of a clock generator "adacgen_new" included in the circuit of Figs. 9.0103AJ-FP.~~

~~Fig. 9.010302 is a graph illustrating how Figs. 9.010302AA-AB are to be assembled. After such assembly, Figs. 9.010302AA-AB provide a circuit drawing of a control output driver "adacdrv_new" included in the circuit of Figs. 9.0103AJ-FP.~~

~~Fig. 9.010303 is a graph illustrating how Figs. 9.010303AA-AB are to be assembled. After such assembly, Figs. 9.010303AA-AB provide a circuit drawing of a control output driver "adacdrvn_new" included in the circuit of Figs. 9.0103AJ-FP.~~

~~Fig. 9.010304 is a graph illustrating how Figs. 9.010304AA-BB are to be assembled. After such assembly, Figs. 9.010304AA-BB provide a circuit drawing of a data latch "adadlat_new" included in the circuit of Figs. 9.0103AJ-FP.~~

~~Fig. 9.0104 is a graph illustrating how Figs. 9.0104AA-DD are to be assembled. After such assembly, Figs. 9.0104AA-DD provide a circuit drawing~~

~~of an analog bias circuit "adabias_new" included in the circuit of Figs. 9.01AA-DH.~~

~~Fig. 9.02 is a graph illustrating how Figs. 9.02AA-DK are to be assembled. After such assembly, Figs. 9.02AA-DK provide a circuit drawing of a Vdd power up detector "pup" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.03 is a graph illustrating how Figs. 9.03AA-BB are to be assembled. After such assembly, Figs. 9.03AA-BB provide a circuit drawing of a master bias source "mbs" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.0301 is a graph illustrating how Figs. 9.0301AA-DJ are to be assembled. After such assembly, Figs. 9.0301AA-DJ provide a circuit drawing of a band gap reference generator "mbs_bgr" included in the circuit of Figs. 9.03AA-BB.~~

~~Fig. 9.0302 is a graph illustrating how Figs. 9.0302AA-DI are to be assembled. After such assembly, Figs. 9.0302AA-DI provide a circuit drawing of a temperature compensated current generator "mbs_cur" included in the circuit of Figs. 9.03AA-BB.~~

~~Fig. 9.0303 is a graph illustrating how Figs. 9.0303AA-CF are to be assembled. After such assembly, Figs. 9.0303AA-CF provide a circuit drawing of a reference current generator "mbs_iref" included in the circuit of Figs. 9.03AA-BB.~~

~~Fig. 9.04 is a graph illustrating how Figs. 9.04AA-CE are to be assembled. After such assembly, Figs. 9.04AA-CE provide a circuit drawing of a voltage regulator "vrg" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.05 is a graph illustrating how Figs. 9.05AA-FE are to be assembled. After such assembly, Figs. 9.05AA-FE provide a circuit drawing of a voltage regulator "vrgtx" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.0501 is a graph illustrating how Figs. 9.0501AA-CD are to be assembled. After such assembly, Figs. 9.0501AA-CD provide a circuit drawing of an operational amplifier without compensation "opampnc" included in the circuit of Figs. 9.05AA-FE.~~

~~Fig. 9.06 is a graph illustrating how Figs. 9.06AA-DD are to be assembled. After such assembly, Figs. 9.06AA-DD provide a circuit drawing of a bias OK detector "biasok" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.07 is a graph illustrating how Figs. 9.07AA-EG are to be assembled. After such assembly, Figs. 9.07AA-EG provide a circuit drawing of an analog port current source "aportcs" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.08 is a graph illustrating how Figs. 9.08AA-CC are to be assembled. After such assembly, Figs. 9.08AA-CC provide a circuit drawing of an analog multiplexer decoder "asl" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.09 is a graph illustrating how Figs. 9.09AA-BB are to be assembled. After such assembly, Figs. 9.09AA-BB provide a circuit drawing of a random clock generator "rcg" included in the circuit of Figs. 9AA-CB.~~

~~Fig. 9.0901 is a graph illustrating how Figs. 9.0901AA-CH are to be assembled. After such assembly, Figs. 9.0901AA-CH provide a circuit drawing of a linear feedback shift register "rcg_sreg" included in the circuit of Figs. 9.09AA-CB.~~

~~Fig. 9.090101 is a graph illustrating how Figs. 9.090101AA-CC are to be assembled. After such assembly, Figs. 9.090101AA-CC provide a circuit drawing of a shift register bit "rcg_sregbit0" included in the circuit of Figs. 9.0901AA-CH.~~

~~Fig. 9.090102 is a graph illustrating how Figs. 9.090102AA-BB are to be assembled. After such assembly, Figs. 9.090102AA-BB provide a circuit drawing of a shift register bit "rcg_sregbit" included in the circuit of Figs. 9.0901AA-CH.~~

~~Fig. 9.0902 is a graph illustrating how Figs. 9.0902AA-FL are to be assembled. After such assembly, Figs. 9.0902AA-FL provide a circuit drawing of a low power oscillator and bias generator "rcg_osc" included in the circuit of Figs. 9.09AA-CB.~~

~~Fig. 9.0903 is a graph illustrating how Figs. 9.0903AA-CC are to be assembled. After such assembly, Figs. 9.0903AA-CC provide a circuit drawing of a clock generator "rcg_clkgen" included in the circuit of Figs. 9.09AA-CB.~~

~~Fig. 10 is a graph illustrating how Figs. 10AA-DD are to be assembled. After such assembly, Figs. 10AA-DD provide a circuit drawing of a pn processor "pnproc" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 10.01 is a graph illustrating how Figs. 10.01AA-DI are to be assembled. After such assembly, Figs. 10.01AA-DI provide a circuit drawing of a digital PN correlator "dcorr" included in the circuit of Figs. 10AA-DI.~~

~~Fig. 10.0101 is a graph illustrating how Figs. 10.0101AA-BG are to be assembled. After such assembly, Figs. 10.0101AA-BG provide a circuit drawing of a PN correlator shift register "dcorr_sreg" included in the circuit of Figs. 10.01AA-DI.~~

~~Fig. 10.010101 is a circuit drawing of a PN correlator bit "dcorr_bit" included in the circuit of Figs. 10.0101AA-BG.~~

~~Fig. 10.01010101 is a circuit drawing of a shift register cell "dcorr_sregbit" included in the circuit of Figs. 10.010101.~~

~~Fig. 10.0102 is a graph illustrating how Figs. 10.0102AA-CN are to be assembled. After such assembly, Figs. 10.0102AA-CN provide a circuit drawing of a correlator bias generator "dcorr_bias" included in the circuit of Figs. 10.01AA-DI.~~

~~Fig. 10.02 is a graph illustrating how Figs. 10.02AA-BE are to be assembled. After such assembly, Figs. 10.02AA-BE provide a circuit drawing of a PN lock detector "pnlockdet" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 10.0201 is a graph illustrating how Figs. 10.0201AA-AB are to be assembled. After such assembly, Figs. 10.0201AA-AB provide a circuit drawing of a counter bit "lockcounterbit" included in the circuit of Figs. 10.02AA-BE.~~

~~Fig. 10.03 is a graph illustrating how Figs. 10.03AA-AB are to be assembled. After such assembly, Figs. 10.03AA-AB provide a circuit drawing of a PN generator clock "pngclk" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 10.04 is a graph illustrating how Figs. 10.04AA-CE are to be assembled. After such assembly, Figs. 10.04AA-CE provide a circuit drawing of a PN generator shift register "pngshr" included in the circuit of Figs. 10 AA-DD.~~

~~Fig. 10.0401 is a circuit drawing of a PN generator shift register cell "pngsreg" included in the circuit of Figs. 10.04AA-CE.~~

~~Fig. 10.0402 is a graph illustrating how Figs. 10.0402AA-CB are to be assembled. After such assembly, Figs. 10.0402AA-CB provide a circuit drawing of a PN generator shift register summer "pngssum" included in the circuit of Figs. 10.04AA-CE.~~

~~Fig. 10.05 is a circuit drawing of a PN controller D type flip-flop "pnddff" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 10.06 is a graph illustrating how Figs. 10.06AA-DH are to be assembled. After such assembly, Figs. 10.06AA-DH provide a circuit drawing of differential and PN encoder "dpenc" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 10.07 is a graph illustrating how Figs. 10.07AA-CD are to be assembled. After such assembly, Figs. 10.07AA-CD provide a circuit drawing of a PSK/FSK generator "fskgen" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 10.0701 is a graph illustrating how Figs. 10.0701AA-AB are to be assembled. After such assembly, Figs. 10.0701AA-AB provide a circuit drawing of a FSK counter bit "fskcbit" included in the circuit of Figs. 10AA-DD.~~

~~Fig. 11 is a graph illustrating how Figs. 11AA-AB are to be assembled. After such assembly, Figs. 11AA-AB provide a circuit drawing of a battery I/O buffer "batalg" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 12 is a graph illustrating how Figs. 12AA-AB are to be assembled. After such assembly, Figs. 12AA-AB provide a circuit drawing of a digital I/O pad buffer "paddig" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 13 is a circuit drawing of a digital input pad buffer "paddigin" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 13.5 is a circuit drawing of a digital input pad buffer "paddigin2" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 14 is a circuit drawing of an analog I/O pad buffer "padalg" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 15 is a graph illustrating how Figs. 15AA-BC are to be assembled. After such assembly, Figs. 15AA-BC provide a circuit drawing of return link configuration control logic "rlconfig" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 16 is a graph illustrating how Figs. 16AA-EH are to be assembled. After such assembly, Figs. 16AA-EH provide a circuit drawing of a temperature sensor "tsn" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 16.01 is a graph illustrating how Figs. 16.01AA-DI are to be assembled. After such assembly, Figs. 16.01AA-DI provide a circuit drawing of an operational amplifier "opamp" included in the circuit of Figs. 16AA-EH.~~

~~Fig. 17 is a graph illustrating how Figs. 17AA-BB are to be assembled. After such assembly, Figs. 17AA-BB provide a circuit drawing of a magnetic field sensor "mag" (a sensor for sensing magnetic fields) included in the circuit of Figs. 6AA-EK.~~

~~Fig. 18 is a graph illustrating how Figs. 18AA-AB are to be assembled. After such assembly, Figs. 18AA-AB provide a circuit drawing of a chip bypass capacitor "bypcap3" included in the circuit of Figs. 6AA-EK.~~

~~Fig. 19 is a graph illustrating how Figs. 19AA-EK are to be assembled. After such assembly, Figs. 19AA-EK provide a circuit drawing of a monolithic semiconductor integrated circuit "LO3BT3F" in accordance with an alternative embodiment of the invention. The integrated circuit of Figs. 19AA-EK is similar to the integrated circuit shown in Figs. 6AA-EK, like component names indicating like components, except that the integrated circuit of Figs. 19AA-EK has no ROM, and is adapted to be connected to external ROM "extrom". The embodiment of Figs. 19AA-EK is particularly useful for test purposes.~~

~~Fig. 20 is a graph illustrating how Figs. 20AA-DF are to be assembled. After such assembly, Figs. 20AA-DF provide a circuit drawing of a data processor "dataproc_t3" to be used in the integrated circuit of Fig. 19 in place of the data processor "dataproc" of Fig. 7.~~

~~Fig. 20.01 is a graph illustrating how Figs. 20.01AA-CB are to be assembled. After such assembly, Figs. 20.01AA-CB provide a circuit drawing of an external ROM "extrom" shown in Figs. 20AA-CB.~~

~~Fig. 20.0101 is a graph illustrating how Figs. 20.0101AA-BB are to be assembled. After such assembly, Figs. 20.0101AA-BB provide a circuit drawing of external ROM control logic "extromctl" included in the circuit of Figs. 20.01AA-CB.~~

~~Fig. 20.0102 is a circuit drawing of an external ROM address interface "extromad" included in the circuit of Figs. 20.01AA-CB.~~

~~Fig. 20.0103 is a graph illustrating how Figs. 20.0103AA-AC are to be assembled. After such assembly, Figs. 20.0103AA-AC provide a circuit drawing of a digital I/O pad buffer "paddigt3" included in the circuit of Figs. 20.01AA-CB.~~

~~Fig. 20.0104 is a circuit drawing of an external ROM databus interface "extromdb" included in the circuit of Figs. 20.01AA-CB.~~

~~Fig. 21 is a circuit schematic illustrating a transmitter switchable between an active mode and a backscatter mode, and employing separate antennas for the active mode and the backscatter mode.~~

~~Fig. 22 is a circuit schematic illustrating a transmitter switchable between an active mode and a backscatter mode, and employing the same antenna for both the active mode and the backscatter mode.~~

~~Fig. 23 is a circuit schematic illustrating low battery detection circuitry.~~

~~Fig. 24 is a circuit schematic illustrating circuitry providing a low power wake up timer.~~

~~Figs. 25-26 provide a flowchart illustrating logic employed for switching between a low power sleep mode, and higher power modes.~~

~~Fig. 27 is a diagram of current versus time illustrating switching between a low power sleep mode, and higher power modes.~~

~~Fig. 28 is a circuit schematic illustrating a Schottky diode detector.~~

~~Fig. 29 is a circuit schematic illustrating a Schottky diode detector in accordance with one embodiment of the invention.~~

~~Fig. 30 is a circuit schematic illustrating a Schottky diode detector in accordance with another embodiment of the invention.~~

~~Fig. 31 is a waveform diagram illustrating the effect of high power radio frequency input levels on Schottky detectors.~~

~~Fig. 32 is a circuit schematic illustrating a high frequency voltage controlled oscillator differential stage.~~

~~Fig. 33 is a waveform diagram illustrating the effect of errors in frequency doubler circuits that necessitates correction, such as by using an integrator and feedback.~~

~~Fig. 34 is a circuit schematic illustrating a frequency doubler circuit that employs an integrator and feedback to solve the problem illustrated in Fig. 33.~~

~~Fig. 35 is a waveform diagram illustrating input and output waves created and employed by a frequency doubler circuit such as the one shown in Fig. 34.~~

~~Fig. 36 is a circuit schematic illustrating a symmetric frequency doubler circuit that does not require an integrator and feedback to solve the problem illustrated in Fig. 33. The frequency doubler circuit of Fig. 36 creates and employs waveforms such as those shown in Fig. 35.~~

~~Fig. 37 is a circuit schematic of an inverter illustrating a power saving technique employed in a pseudo random number generator embodying one aspect of the invention.~~

~~Fig. 38 is a cross-sectional view illustrating a step of a process of manufacturing a Schottky diode.~~

~~Fig. 39 is a cross-sectional view illustrating a step subsequent to the step of Fig. 38.~~

~~Fig. 40 is a cross-sectional view illustrating a step subsequent to the step of Fig. 39.~~

~~Fig. 41 is a cross-sectional view illustrating a step subsequent to the step of Fig. 40.~~

~~Fig. 42 is a top view illustrating a step subsequent to the step of Fig. 41 and showing parallel connection of some Schottky diodes of a plurality of Schottky diodes.~~

~~Fig. 43 is a top view illustrating a step subsequent to the step of Fig. 41 in accordance with an alternative embodiment of the invention and showing parallel connection of all Schottky diodes of a plurality of Schottky diodes.~~

~~Fig. 44 is a cross-sectional view illustrating a step of an alternative process of manufacturing a Schottky diode.~~

~~Fig. 45 is a cross-sectional view illustrating a step subsequent to the step of Fig. 44.~~

~~Fig. 46 is a cross-sectional view illustrating a step subsequent to the step of Fig. 45.~~

~~Fig. 47 is a cross-sectional view illustrating a step subsequent to the step of Fig. 46.~~

~~Fig. 48 is a simplified circuit schematic of a quick bias AC-coupled video amplifier included in the integrated circuit.~~

~~Fig. 49 is a plot of voltage versus angular frequency illustrating selection of components to realize a desired high pass roll off frequency in the amplifier of Fig. 48.~~

~~Fig. 50 is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and an active transmitter.~~

~~Fig. 51 is a simplified circuit schematic illustrating circuitry included in the active transmitter of Fig. 50 in accordance with one aspect of the invention.~~

~~Fig. 52 is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and a backscatter transmitter.~~

~~Fig. 53 is a simplified circuit schematic illustrating sharing of a single antenna by both a Schottky detector and a backscatter transmitter in accordance with an alternative embodiment of the invention.~~

~~Fig. 54 is a graph of voltage versus time illustrating a method of determining when frequency lock has occurred.~~

~~Fig. 55 is a flowchart illustrating a top level of code stored in ROM in the integrated circuit.~~

~~Figs. 56A and B define a flowchart illustrating a command processing routine performed by the integrated circuit.~~

~~Figs. 57A and B define a flowchart illustrating steps performed by the integrated circuit in response to an Identify command received from the interrogator in which the interrogator requests, via radio frequency command, identification of an integrated circuit.~~

~~Fig. 58 is a flowchart illustrating steps performed to initialize the interrogator.~~

~~Fig. 59 is a flowchart illustrating steps performed when the interrogator sends a command to the integrated circuit.~~

~~Fig. 60 is a flowchart illustrating steps performed by the interrogator in issuing an Identify command.~~

~~Fig. 61 is a simplified circuit diagram of a digital clock recovery loop including a start-up circuit including a counter, a voltage controlled oscillator, a charge pump and loop filter, and a state machine. The start-up circuit and counter determine when clock frequency is close to a desired value.~~

~~Fig. 62 is a plot of frequency produced by a voltage controlled oscillator versus control voltage applied to the voltage controlled oscillator.~~

~~Fig. 63 is a timing diagram showing when the start-up circuit of Fig. 61 issues pump up signals to increase the control voltage applied to the voltage controlled oscillator.~~

~~Fig 64 is a state diagram illustrating the design of the state machine of Fig. 61.~~

~~Figs. 65-70 illustrate steps used in designing a state machine that implements the state diagram of Fig. 64. Fig. 65 illustrates flip-flops having outputs representing in binary form the various states of the state diagrams and having inputs representing next state values. Fig. 66 is a state table. Figs. 67 and 68 are Karnaugh maps used to derive minimum logic circuitry needed to derive circuit output functions and flip-flop input functions.~~

~~Fig. 71 is a simplified timing diagram illustrating operation of the state machine.~~

~~Fig. 72 is a table illustrating step sizes produced by the start-up circuit and the state machine.~~